IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No. 10/537,195	***Confirmation No. 3437***
Filed: June 2, 2005	
Applicants: Martin Beale	This Amendment and Response was electronically filed on June 21, 2010 using EFS-Web.
Title: **SUPPORT OF PLURAL CHIP RATES IN A CDMA SYSTEM**	
Art Unit: 2618	
Examiner: Pablo N. Tran	
Attorney Docket: 9010/96586 (02-0093) SO2B4004US99	
Customer No.: 22242	

BRIEF IN SUPPORT OF PRE-APPEAL REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed February 19, 2010, please enter the following brief in support of the co-filed Pre-Appeal Request for Review. A Notice of Appeal is also submitted herewith.

Claims 1-5, 9-15, 23-28, 32-39, 46-51, 55-61, and 91-92, and 94-95 were rejected under 35 U.S.C. 102(a) as being anticipated by Nasshan et al. (EP0876008) ("Nasshan") and claims 6-9, 17-22, 29-32, 40-45, 52-55, and 63-68 were rejected under 35 U.S.C. 103(a) as being unpatentable over Nasshan in view of Chuah (US Pat. No. 6,115,390) ("Chuah"). Applicants respectfully submit that at least some of these rejections are based upon clear error.

I. Clear Error: Nasshan does not teach or suggest allocating, on a per time slot basis, a time slot at a first chip rate (selected from a plurality of chip rates) based on the chip rate capability of the user equipment

Our claim 1 reads as follows:

> A method for supporting of a plurality of chip rates in a code division multiple access (CDMA) system between a plurality of user equipment (UE) sharing a plurality of timeslots in a frame, the method comprising:
>
> allocating to a UE at least a first timeslot of the plurality of timeslots in the frame at a first chip rate of the plurality of chip rates based on a chip rate capability of the UE on a per timeslot basis.

The word "chip" as appears in this claim is a well-recognized term of art and refers to a pulse of a direct-sequence spread spectrum (DSSS) code, such as a pseudo-noise code sequence used in direct-sequence code division multiple access (CDMA). In a binary direct-sequence system, for example, each "chip" is typically a rectangular pulse of +1 or –1 amplitude that is multiplied by a data sequence and by a carrier waveform to yield the transmitted signal.

Accordingly, "chips" are not "bits." In fact, chips are *called* "chips" in order "to *avoid* confusing them with message bits."[1]

The expression "chip rate," in turn, refers to the number of pulses per second (i.e., chips per second) at which the code sequence is transmitted/received. As such, "chip rate" does not equate to "bit rate."

[1] *See*, for example, Wikipedia at http://en.wikipedia.org/wiki/Chip_(CDMA); emphasis added.

The Nasshan prior art reference makes some reference to "chips" in the context of his CDMA application setting, and makes frequent reference to "bit rates" as his invention is specifically directed to adapting the bit rate of a communication link of a digital mobile communication system[2]. Nasshan, however, makes no reference whatsoever to "chip rates" and in particular makes no reference to making any kind of decision based upon the "chip rate capability" of an end user platform.

The Examiner rests his position upon the following analysis of Nasshan:

> In repose to the Applicant, Nasshan disclose a mechanism for adapting a bit rate in a CDMA communication system wherein based upon the capabilities of the receiving user device and selecting a number of timeslots in accordance with the required bit rate and the receiving capabilities and allocating the bits rate to the selected time slot (see pg. 3/ln. 7-pg. 3/ln. 15). Therefore, the rejection is proper.

This position, however, simply echoes what we have stated above – Nasshan describes adapting a "bit rate." Regardless of how many times one might confirm this insight, however, this finding stops well short of anticipating the making of a decision based upon the chip rate capability of an end user platform as, at the least, "bit rates" and "chip rates" are two distinct and separate things. With all due respect, such an approach, in effect, confuses apples with oranges.

Simply put, Nasshan clearly and unequivocally fails to teach or suggest "allocating to a UE at least a first timeslot of the plurality of timeslots in the frame at a first chip rate of the plurality of chip rates based on a chip rate capability of the UE on a per timeslot basis" as required by our claim 1.

Our other independent claims, 24, 47, 91, 92, 94, and 95 can be similarly distinguished.

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[2] *See Naashan* at paragraph 0001.

Accordingly, we respectfully submit that it is clear error to view Nasshan as anticipating our claims.

Respectfully submitted,

FITCH, EVEN, TABIN & FLANNERY

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Steven G. Parmelee
Registration No. 28,790

120 South LaSalle Street, Suite 1600
Chicago, Illinois 60603-3406
Telephone (312) 577-7000
Facsimile (312) 577-7007